

30V P-Ch Power MOSFET

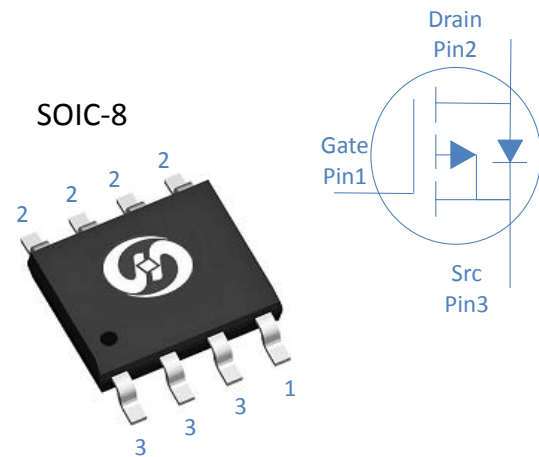
Feature

- ◇ High Speed Power Switching, Logic Level
- ◇ Enhanced Avalanche Ruggedness
- ◇ 100% UIS Tested, 100% Rg Tested
- ◇ Lead Free, Halogen Free

V_{DS}		-30	V
$R_{DS(on),typ}$	$V_{GS}=10V$	6	$m\Omega$
$R_{DS(on),typ}$	$V_{GS}=4.5V$	9	$m\Omega$
I_D (Silicon Limited)		-15	A

Application

- ◇ Hard Switching and High Speed Circuit
- ◇ DC/DC in Telecoms and Industrial



Part Number	Package	Marking
HTS075P03	SOIC-8	TS075P03

Absolute Maximum Ratings at $T_j=25^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	$T_C=25^\circ\text{C}$	-15	A
		$T_C=100^\circ\text{C}$	-11	
Drain to Source Voltage	V_{DS}	-	-30	V
Gate to Source Voltage	V_{GS}	-	± 20	V
Pulsed Drain Current	I_{DM}	-	-60	A
Avalanche Energy, Single Pulse	E_{AS}	$L=0.1\text{mH}, T_C=25^\circ\text{C}$	31.25	mJ
Power Dissipation	P_D	$T_A=25^\circ\text{C}$	3	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 175	$^\circ\text{C}$

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Thermal Resistance Junction-Case	$R_{\theta JC}$	25	$^\circ\text{C/W}$

Electrical Characteristics at $T_J=25^{\circ}\text{C}$ (unless otherwise specified)
Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.0	-2.0	-3.0	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS}=0V, V_{DS}=-24V, T_J=25^{\circ}\text{C}$	-	-	-1	μA
		$V_{GS}=0V, V_{DS}=-20V, T_J=125^{\circ}\text{C}$	-	-	-10	
Gate to Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-12A$	-	6	7.5	m Ω
		$V_{GS}=-4.5V, I_D=-9A$	-	9	12	
Transconductance	g_{fs}	$V_{DS}=-5V, I_D=-12A$	-	28	-	S
Gate Resistance	R_G	$V_{GS}=15mV, V_{DS}=0V, f=1MHz$	-	3	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=-15V, f=1MHz$	-	15545	-	pF
Output Capacitance	C_{oss}		-	3776	-	
Reverse Transfer Capacitance	C_{rss}		-	3507	-	
Total Gate Charge	$Q_g (10V)$	$V_{DD}=-15V, I_D=-10A, V_{GS}=-10V$	-	56	-	nC
	$Q_g (4.5V)$		-	35	-	
Gate to Source Charge	Q_{gs}		-	15	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	18	-	
Turn on Delay Time	$t_{d(on)}$		-	26	-	
Rise time	t_r	$V_{DD}=-15V, I_D=-1A, V_{GS}=-10V,$	-	22	-	
Turn off Delay Time	$t_{d(off)}$	$R_G=2.7\Omega,$	-	75	-	
Fall Time	t_f		-	15	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_F=-3A$	-		-1.2	V
Reverse Recovery Time	t_{rr}	$I_F=-3.6A, dI_F/dt=100A/\mu s$	-	52	-	ns
Reverse Recovery Charge	Q_{rr}		-	60	-	nC

Fig 1. Typical Output Characteristics

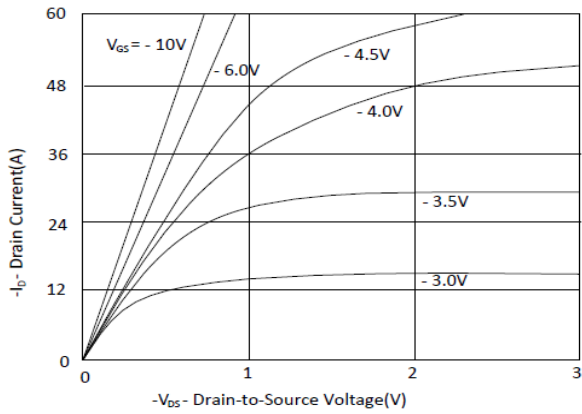


Figure 2. On-Resistance vs. Gate-Source Voltage

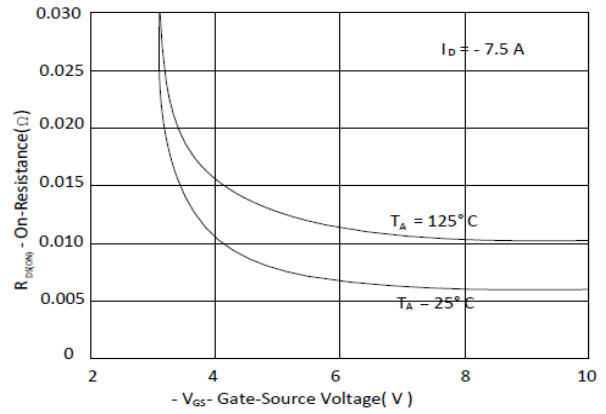


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

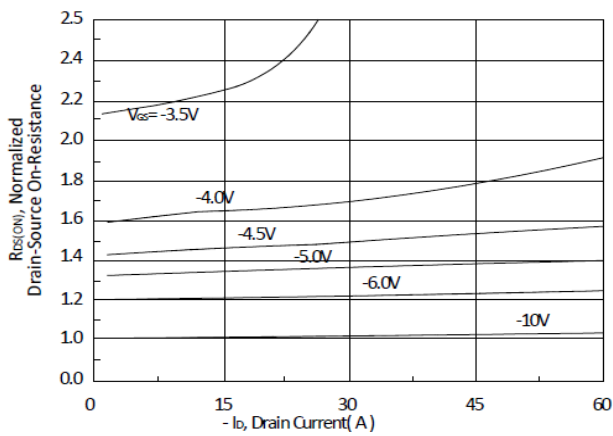


Figure 4. Normalized On-Resistance vs. Junction Temperature

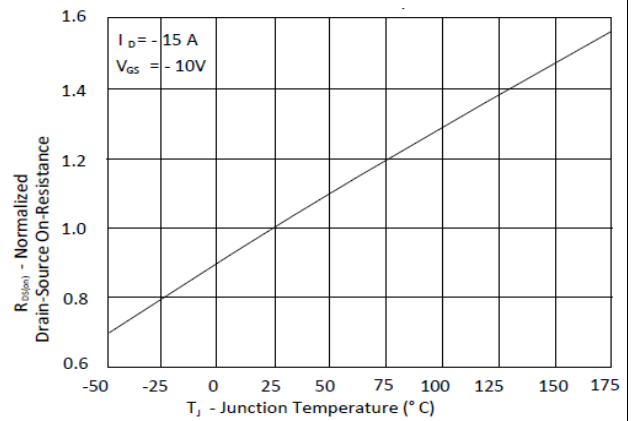


Figure 5. Typical Transfer Characteristics

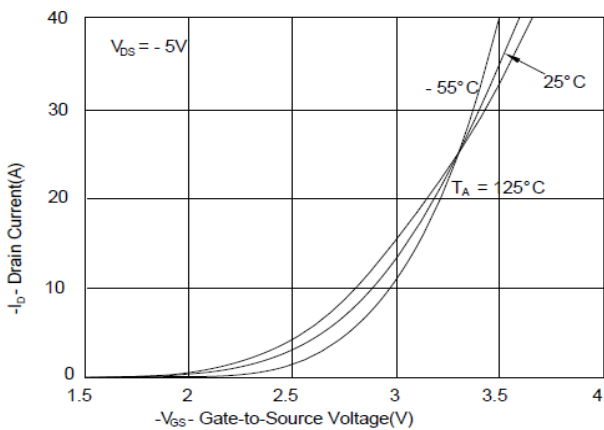


Figure 6. Typical Source-Drain Diode Forward Voltage

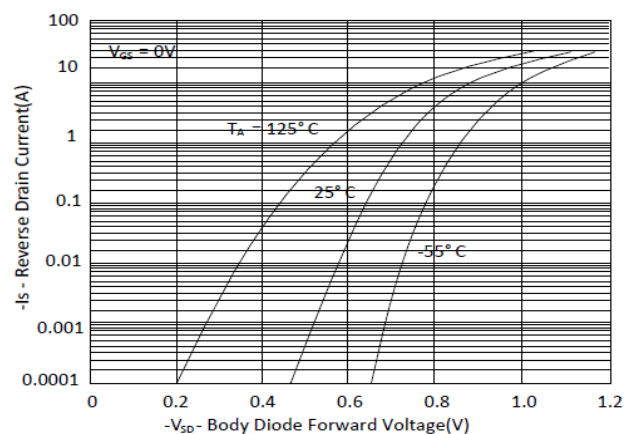


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

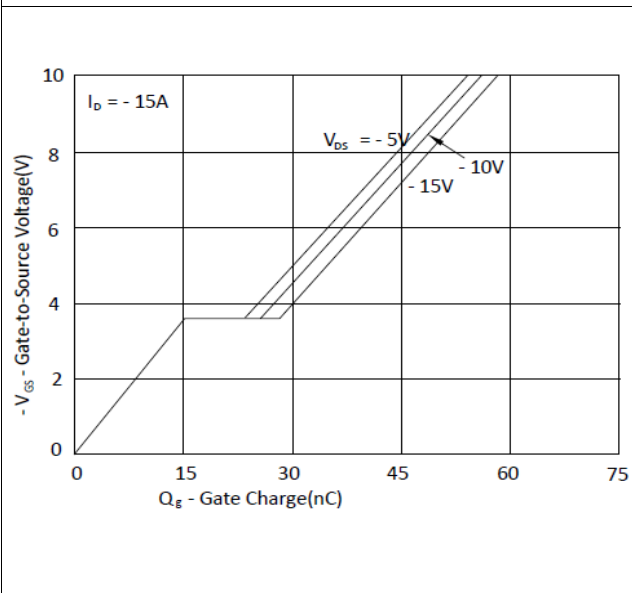


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

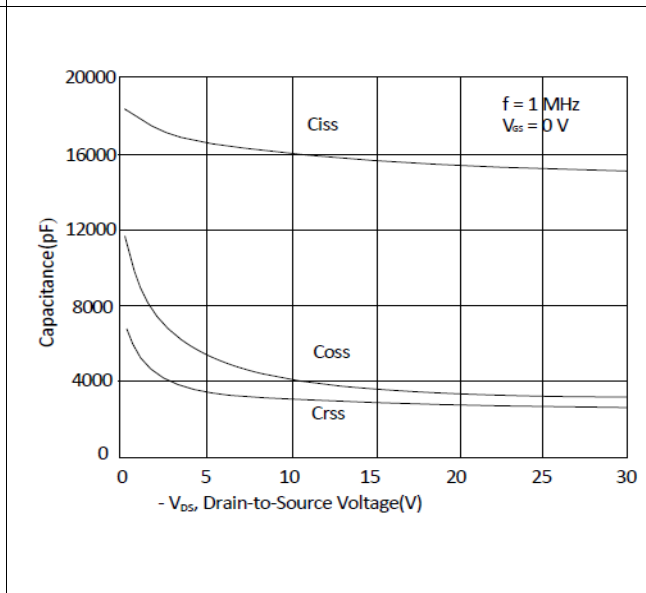


Figure 9. Maximum Safe Operating Area

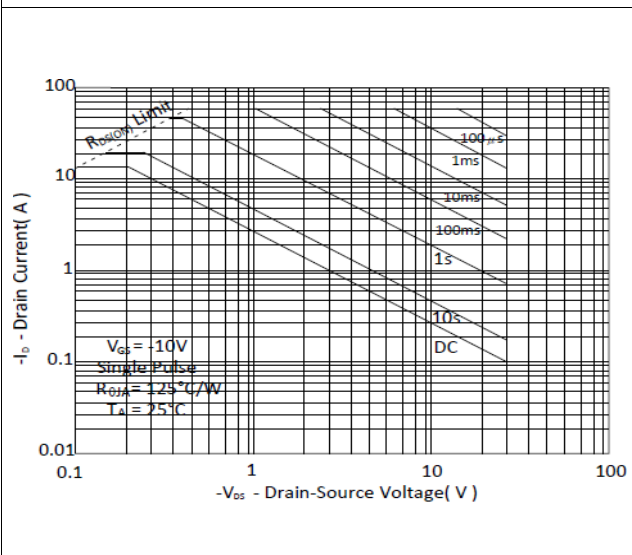


Figure 10. Single Pulse Maximum Dissipation

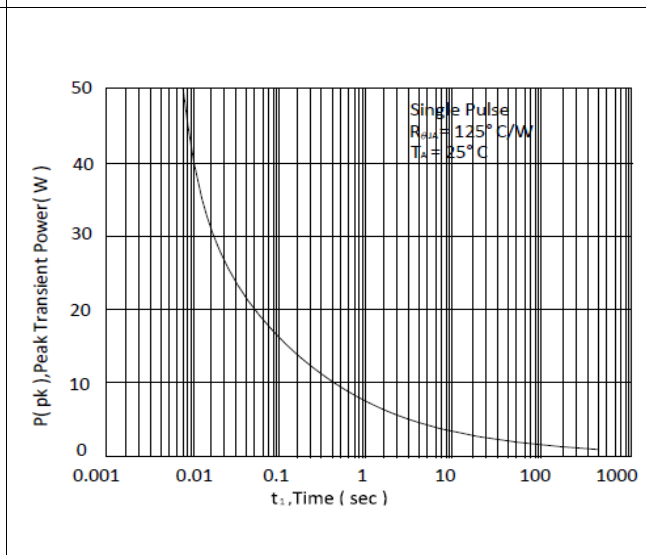
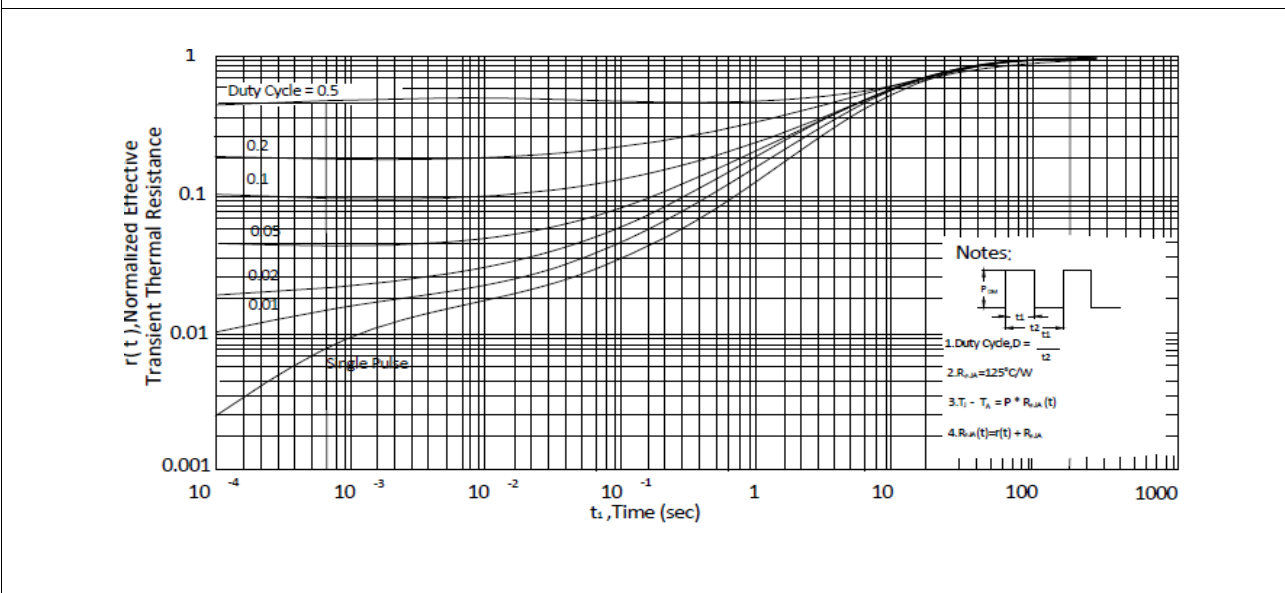
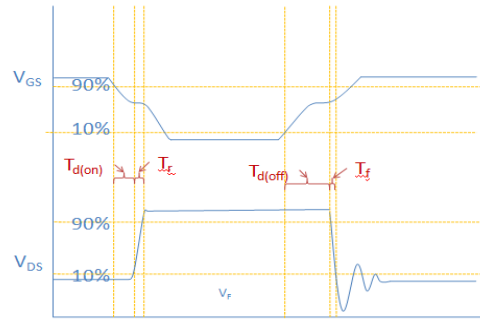
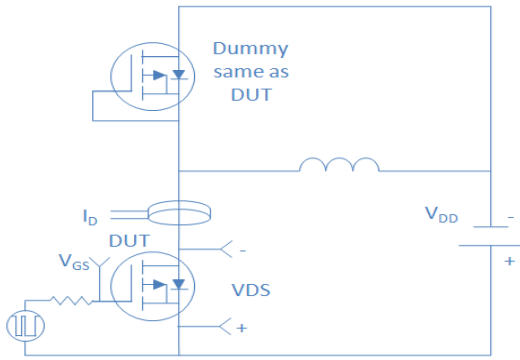


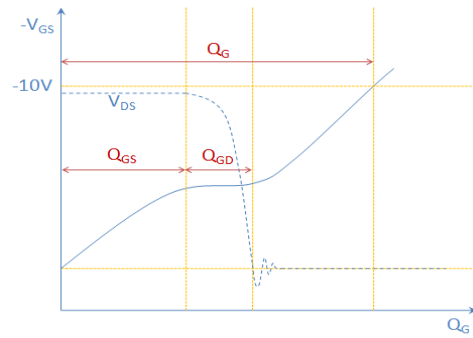
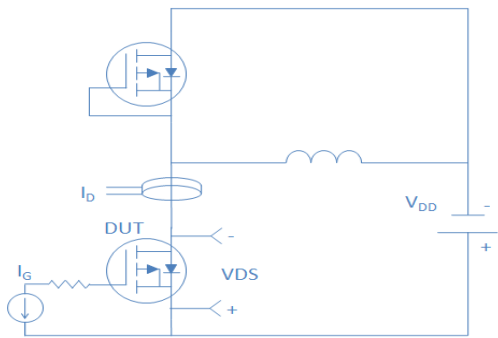
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



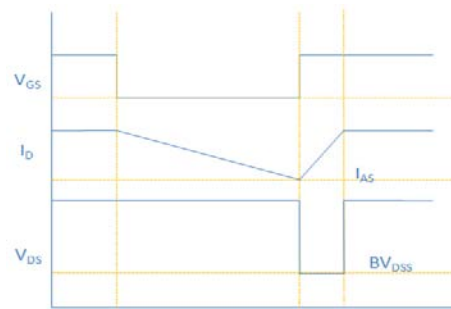
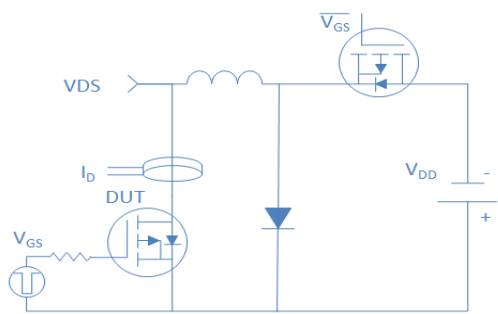
Inductive switching Test



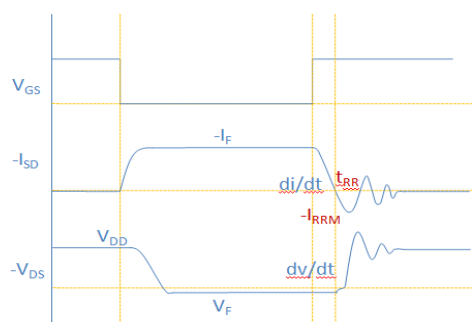
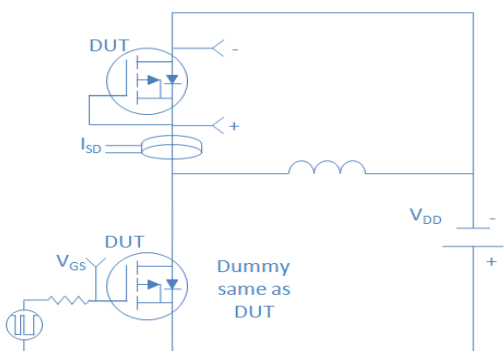
Gate Charge Test



Uclamped Inductive Switching (UIS) Test

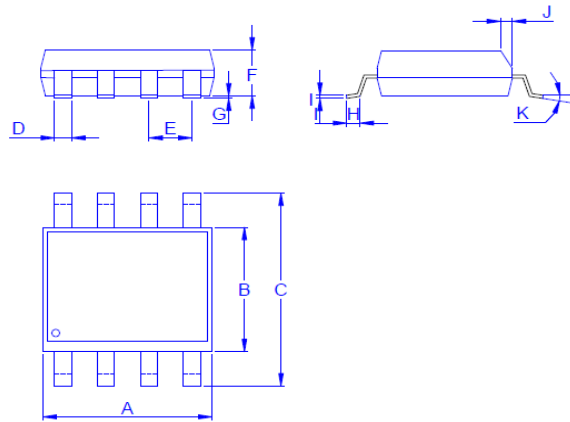


Diode Recovery Test



Package Outline

SOIC-8, 8leads



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
in.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°